WHAT IS CLAIMED IS:

1. An MPEG decoder comprising:

a packetized elementary stream (PES) interface capable of receiving a plurality of packetized elementary streams associated with a single video program;

a presentation time stamp (PTS) detection circuit capable of detecting presentation time stamps in said packetized elementary streams and extracting said presentation time stamps therefrom; and

a selection circuit capable of selecting presentation time stamps associated with a first one of said plurality of packetized elementary streams and transmitting said selected presentation time stamps to a clock generation circuit, wherein said clock generation circuit generates a first reference clock signal used by a first decoder to decode said first packetized elementary stream.

2. The MPEG decoder as set forth in Claim 1 wherein said clock generation circuit further generates a second reference clock signal synchronized to said first reference clock signal and wherein said second reference clock signal is used by a second decoder to decode a second packetized elementary stream in synchronization with said first packetized elementary stream.

3. The MPEG decoder as set forth in Claim 2 wherein said selected presentation time stamps are video presentation times stamps and said first decoder is a video decoder.

4. The MPEG decoder as set forth in Claim 3 wherein said second decoder is an audio decoder.

5. The MPEG decoder as set forth in Claim 2 wherein said selected presentation time stamps are audio presentation times stamps and said first decoder is an audio decoder.

6. The MPEG decoder as set forth in Claim 5 wherein said second decoder is a video decoder.

7. The MPEG decoder as set forth in Claim 2 said clock generation circuit generates said second reference clock signal by synchronizing presentation time stamps associated with said second packetized elementary stream with said selected presentation time stamps associated with said first packetized elementary stream.

8. A digital video recorder capable of playing back a recorded television program stored as packetized elementary streams, said digital video recorder comprising:

a video processor capable of receiving an incoming television program and converting said incoming television program to a baseband video signal capable of being displayed on a television set coupled to said digital video recorder;

a storage disk capable of storing said incoming television program as packetized elementary streams during recording; and

an MPEG decoder comprising:

a packetized elementary stream (PES) interface capable of receiving a plurality of packetized elementary streams associated with said recorded television program from said storage disk during playback;

a presentation time stamp (PTS) detection circuit capable of detecting presentation time stamps in said packetized elementary streams and extracting said presentation time stamps therefrom; and

a selection circuit capable of selecting presentation time stamps associated with a first one of said plurality of packetized elementary streams and transmitting

said selected presentation time stamps to a clock generation circuit, wherein said clock generation circuit generates a first reference clock signal used by a first decoder to decode said first packetized elementary stream.

9. The digital video recorder as set forth in Claim 8 wherein said clock generation circuit further generates a second reference clock signal synchronized to said first reference clock signal and wherein said second reference clock signal is used by a second decoder to decode a second packetized elementary stream in synchronization with said first packetized elementary stream.

10. The digital video recorder as set forth in Claim 9 wherein said selected presentation time stamps are video presentation times stamps and said first decoder is a video decoder.

11. The digital video recorder as set forth in Claim 10 wherein said second decoder is an audio decoder.

12. The digital video recorder as set forth in Claim 9 wherein said selected presentation time stamps are audio presentation times stamps and said first decoder is an audio decoder.

13. The digital video recorder as set forth in Claim 12 wherein said second decoder is a video decoder.

14. The digital video recorder as set forth in Claim 9 said clock generation circuit generates said second reference clock signal by synchronizing presentation time stamps associated with said second packetized elementary stream with said selected presentation time stamps associated with said first packetized elementary stream.

15. For use in a digital video recorder, a method for decoding a television program stored in MPEG format:

receiving in an MPEG decoder a plurality of packetized elementary streams associated with the stored television program;

detecting presentation time stamps in the packetized elementary streams;

extracting the presentation time stamps from the packetized elementary streams;

selecting presentation time stamps associated with a first one of the plurality of packetized elementary streams; and

generating from the selected presentation time stamps a first reference clock signal used by a first decoder to decode the first packetized elementary stream.

16. The method as set forth in Claim 15 further comprising the step of generating a second reference clock signal synchronized to the first reference clock signal, wherein the second reference clock signal is used by a second decoder to decode a second packetized elementary stream in synchronization with the first packetized elementary stream.

17. The method as set forth in Claim 14 wherein the selected presentation time stamps are video presentation times stamps and the first decoder is a video decoder.

18. The method as set forth in Claim 17 wherein the second decoder is an audio decoder.

19. The method as set forth in Claim 16 wherein the selected presentation time stamps are audio presentation times stamps and the first decoder is an audio decoder.

20. The method as set forth in Claim 19 wherein the second decoder is a video decoder.

21. The method as set forth in Claim 16 wherein the step of generating a second reference clock signal comprises the sub-step of synchronizing presentation time stamps associated with the second packetized elementary stream with the selected presentation time stamps associated with the first packetized elementary stream.